Paper No. 43

THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

UNITED STATES PATENT AND TRADEMARK OFFICE

_____

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

_____

Ex parte ELWYN P. M. WAKEFIELD,
and CHRISTOPHER P.H. WALKER

_____

Appeal No. 96-2243
Application 08/327,447[1]

_____

HEARD: JUNE 9, 1999

_____

Before KRASS, HECKER and LALL, ***Administrative Patent Judges***.

HECKER, ***Administrative Patent Judge.***

DECISION ON APPEAL

[1] Application for patent filed October 21, 1994. According to appellants, this application is a continuation of Application 08/074,984, filed June 10, 1993, now abandoned, which is a continuation of Application 07/808,531, filed December 16, 1991, now abandoned, which is a continuation of Application 07/557,940, filed July 25, 1990, now Patent No. 5,073,816, issued December 17, 1991.

This is a decision on appeal from the final rejection of claims 19 through 27 and 30 through 39, all of the claims pending in the present application.

The invention relates to a package for semiconductor chips. In particular, referring to Figures 1 and 2, a semi-conductor chip package 2 is shown with four chips 4. A thin printed circuit 8 (a first level interconnect), contains conductive tracks 20, and overlies the chips 4. Each end 10 of the printed circuit 8 contains outer leads 12 which extend outside the chip package 2. Bond wires 38 (a second level interconnect), connect each chip to the tracks 20 on the upper side of printed circuit 8.

Representative independent claims 19 and 30 are reproduced as follows:

19. A semiconductor device comprising:

at least one semiconductor chip, the or each semiconductor chip having a plurality of chip bonding pads,

a first level interconnect comprising a printed circuit which overlies the at least one semiconductor chip and is disposed adjacent to the chip bonding pads of the at least one semiconductor chip, the printed circuit having contacts which are located on a side of the printed circuit remote from the or each semiconductor chip and which overlie the at least one semiconductor chip, and

a second level interconnect comprising means for electrically connecting the chip bonding pads to selected contacts on the printed circuit,

the first interconnect being between the second level interconnect and the or each semiconductor chip.

30. A semiconductor device comprising at least one semiconductor chip, a package which encloses the at least one semiconductor chip and a printed circuit which overlies and is electrically connected to the at least one semiconductor chip in the package and extends externally of the package to provide a plurality of outer leads.

The Examiner relies on the following references:

Fukuta et al. (Fukuta)	4,751,482	June 14, 1988
Kishida	4,941,033 (filed Mar. 24, 1989)	July 10, 1990
Carlson et al. (Carlson)	4,953,005 (filed Apr. 15, 1988)	Aug. 28, 1990

Claims 19 through 27[2] stand rejected under 35 U.S.C. § 103 as being unpatentable over Kishida in view of Fukuta.

Claims 30 through 32 stand rejected under 35 U.S.C.

[2] Claims 25 through 27 are not specifically mentioned by the Examiner in the Office Action and Answer, however Appellants have assumed that the Examiner intended to include claims 25 through 27 in the 35 U.S.C. § 103 rejection over Kishida in view of Fukuta, thus we will treat them likewise.

§ 102(b)[3] as anticipated by or, in the alternative, under 35 U.S.C. § 103 as obvious over Kishida.

Claim 33 stands rejected under 35 U.S.C. § 103 as being unpatentable over Kishida in view of Fukuta.

Claims 34 through 39 stand rejected under 35 U.S.C. § 103 as being unpatentable over Kishida in view of Fukuta and Carlson.

Rather than reiterate the arguments of Appellants and the Examiner, reference is made to the brief, reply brief and answer for the respective details thereof.

OPINION

We will not sustain the rejection of claims 19 through 27 and 30 through 39 under 35 U.S.C. § 103, nor the rejection of claims 30 through 32 under the alternative 35 U.S.C. § 102(e) rejection.

The Examiner has failed to set forth a ***prima facie*** case. It is the burden of the Examiner to establish why one

[3] Kishida's patent date (July 10, 1990) does not qualify under 35 U.S.C. § 102(b) since it is less than one year prior to Appellants' effective filing date of July 25, 1990. We will assume 35 U.S.C. § 102(e) is being used since Kishida's filing date of March 24, 1989 is prior to Appellants' foreign priority date of August 14, 1989.

having ordinary skill in the art would have been led to the claimed invention by the reasonable teachings or suggestions found in the prior art, or by a reasonable inference to the artisan contained in such teachings or suggestions. ***In re Sernaker***, 702 F.2d 989, 995, 217 USPQ 1, 6 (Fed. Cir. 1983). "Additionally, when determining obviousness, the claimed invention should be considered as a whole; there is no legally recognizable 'heart' of the invention." ***Para-Ordnance Mfg. v. SGS Importers Int'l, Inc.***, 73 F.3d 1085, 1087, 37 USPQ2d 1237, 1239 (Fed. Cir. 1995) (***citing W. L. Gore & Assocs., Inc. v. Garlock, Inc.***, 721 F.2d 1540, 1548, 220 USPQ 303, 309 (Fed. Cir. 1983), ***cert. denied***, 469 U.S. 851 (1984)).

With regard to the rejection of claims 19 through 27 under 35 U.S.C. § 103 as being unpatentable over Kishida in view of Fukuta, Appellants argue on page 6 of the brief that Kishida and Fukuta fail to disclose

> [T]he first level interconnect comprising the printed circuit lies between the second level interconnect and the semiconductor chip or chips and the contacts on the printed circuit which are connected to the chip bonding pads by the means for electrical connection are located on the side of the

> printed circuit which is remote from the semiconductor chip or chips.

The Examiner responds that "Kishida is deemed to teach a first level interconnect 41 formed between chip 2 and a second level interconnect formed in printed circuit 4." (Answer at page 6).

The Examiner has repeatedly relied on Figure 7 of Kishida, and we will assume the above comments are likewise directed to this Figure. Noting that element 41 is not labeled in Figure 7, we have located element 41 in Figure 1A as being on the lower surface of wiring film 4 (i.e. printed circuit 4). Column 2, lines 48 and 49, designate 41 as a terminal. We are reluctant to deem 41 as an interconnect as claimed by Appellants. However, if 41 is seen as the first level interconnect as proposed by the Examiner, the Examiner would then have us read the second level interconnect as "formed in printed circuit 4." Again, absent sufficient labeling in Figure 7, we understand this to mean the equivalent to wiring 43 in Figure 1A. Granting these designations by the Examiner, we fail to see how the "second level interconnect compris[es] means for electrically

connecting the chip [2] bonding pads to selected contacts on the printed circuit" as recited in claim 19. Figure 7 shows that wiring 43 (i.e. second level interconnect) connects to a terminal (equivalent to 42 in Figure 1A) on the printed circuit board 4, not chip 2 bonding pads. Even if the terminal (e.g. 42) were considered as part of wiring 43, it (the second level interconnect) still does not connect to chip 2 bonding pads,
but rather, through additional elements, to chip 6 (or possibly chip 1).

In a slight variation of this rejection, the Examiner's original rejection designated printed circuit 4 as the first level interconnect. Here again, we fail to see how the claim language is met. In particular, where is the second level interconnect that connects to chip 2 bonding pads on the one hand, to printed circuit 4 contacts which are located on the other side (away from chip 2) on the other hand?

We agree with Appellants that the Examiner has not shown how Kishida reads on the claim 19 language, nor can we

extrapolate any reasoning which would establish such a correspondence. For these reasons, we will not sustain the 35 U.S.C. § 103 rejection of claim 19, and likewise dependent claims 20 through 27 which also contain the limitations discussed supra.

Turning to claim 30, Appellants argue:

> The Applicants do not agree with the Examiner's position that the printed circuit of claim 30 may "extend externally" via an "auxiliary means". (Reply Brief at page 3.)
>
> While the pin (12,13) [of Kishida] may extend the "electrical circuit," it cannot be interpreted to extend the wiring film when in fact the pin (12,13) is a separate and distinct element. (Reply Brief at page 5)

Looking at claim 30 we see the following language:

> and a printed circuit which overlies and is electrically connected to the at least one semiconductor chip in the package and extends externally of the package . . . . (emphasis added)

The Examiner contends that:

> A printed circuit may "extend externally" via auxiliary connection means that by way of a terminal such as 32 forms an external connection extending externally thereto which Kishida shows. Claim 30 fails to recite that the printed circuit is located on the outside of the package. (Answer at page 6)

We agree with the Appellants, the pins of Kishida are not part of the printed circuit, and the printed circuit **is** claimed to extend externally of the package. For these reasons we will not sustain the 35 U.S.C. § 102 or 35 U.S.C. § 103 rejections of claim 30, and likewise the rejection of dependent claims 31 through 33 which contain the same limitation discussed supra.

Independent claim 34 contains the same limitation as discussed with regard to claim 30 (i.e. printed circuit which extends externally of the package), and we will therefore not sustain the 35 U.S.C. § 103 rejection of this claim. Likewise, we will not sustain this rejection of dependent claims 35 through 39 which contain the same limitation.

We have not sustained the rejection of claims 30 through 32 under 35 U.S.C. § 102, nor the rejection of claims 19 through 27 and 30 through 39 under 35 U.S.C. § 103. Accordingly, the Examiner's decision is reversed.

REVERSED

ERROL A. KRASS Administrative Patent Judge	)	
STUART N. HECKER Administrative Patent Judge	)	BOARD OF PATENT APPEALS AND INTERFERENCES
PARSHOTAM S. LALL Administrative Patent Judge	)	

SNH/cam

Kenneth L. Cage, Esq.
McDermott, Will & Emery
1850 K Street, N.W., Suite 500
Washington, DC 20006-2296